15. (Once Amended) A computer-readable medium containing a rules checker computer program, the computer program evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:

code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

16. (Once Amended) The computer-readable medium of claim 15, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the code comprising:

a first code segment which processes the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths;

a second code segment which utilizes the first numerical value to access first and second threshold values stored in a memory device in communication with the computer;

a third code segment which determines noise levels on the input terminals; and

a fourth code segment which compares the determined noise levels with the threshold values read out of the memory device and uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

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17. (Once Amended) The computer-readable medium of claim 16, wherein the first code segment includes model generating code which generates a first model of the gate in order to process the widths of the P and N field effect transistors, the first model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the second code segment to access the first and second threshold values stored in the memory device, wherein when the first and second inputs are high, the third code segment determines noise levels on the first and second inputs and wherein the fourth code segment compares the determined noise levels to the first and second threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the first model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first model, the program determines that the gate has an acceptable immunity to noise.

18. (Once Amended) The computer-readable medium of claim 17, wherein the model generating code generates a second model of the gate, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the second code segment to access a third and fourth threshold values stored in the memory device, wherein the third code segment determines noise levels on the first and second inputs when the first and second inputs are low and wherein the fourth code segment compares the determined noise levels to the third and fourth threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the program determines that the gate has an acceptable noise immunity.

19. (Once Amended) The computer-readable medium of claim 18, wherein the model generating code generates a third model of the gate, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the second code segment to access fifth and sixth threshold values stored in the memory device, wherein when the first input is high, the third code segment determines the noise level on the first input and wherein the fourth code segment compares the determined noise level to the fifth threshold value, and wherein when the first input is low, the third code segment determines the noise level on the

first input and wherein the fourth code segment compares the determined noise level to the sixth threshold value, the fourth code segment using the results of the comparison operations to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the program determines that the gate has an acceptable noise immunity.

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20. (Once Amended) The computer-readable medium of claim 19, wherein the model generating code generates a fourth model of the gate, the fourth model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, the fourth ratio corresponding to a fourth numerical value, the fourth numerical value being used by the second code segment to access seventh and eighth threshold values stored in the memory device, wherein when the second input is low, the third code segment determines the noise level on the second input and wherein the fourth code segment compares the measured noise level to the seventh threshold value, and wherein when the second input is high, the third code segment determines the noise level on the second input and wherein the fourth code segment compares the measured noise level to the eighth threshold value, the fourth code segment using the results of the comparison to determine whether or not the gate meets acceptable noise immunity requirements with respect to the fourth model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first, second, third and fourth models, the program determines that the gate has an acceptable noise immunity.